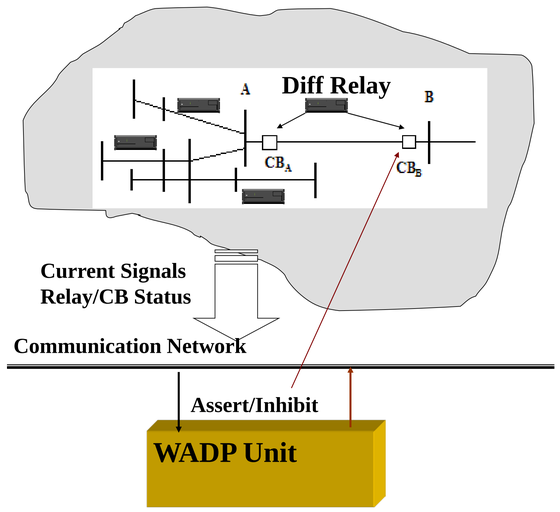
A Wide Area Differential Protection Scheme based on Current Phasors

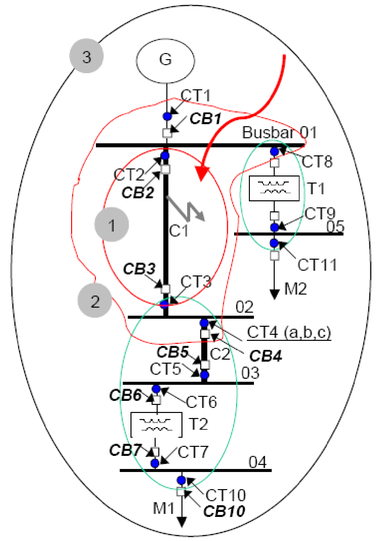
P.McLaren, J. Tang, M.Steurer, R.Meeker, H. Ravindra
Center for Advanced Power Systems (CAPS) at Florida State University

A Power System Region



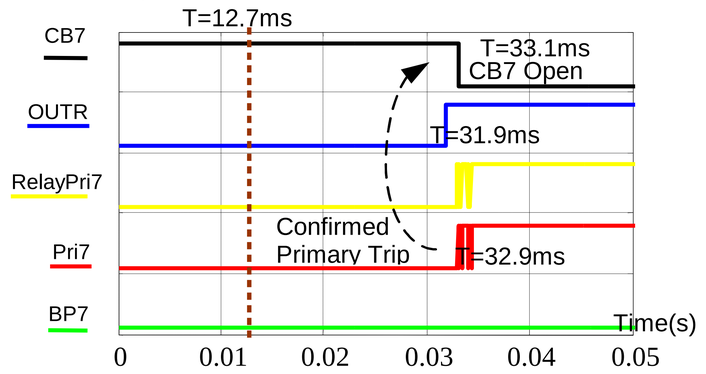
The Back-up Principle

- Current Phasors are required from each node
- Set up differential rings (super nodes) around circuit elements such as 1, 2 and 3.
- The protection system is like a multi-busbar protection with overlapping and interlocking zones.
- Under normal conditions, all Diff Rings are conserved/inactive
- The fault position changes the conservation property of Diff Rings. Some become active and some still stay inactive.
- If a ring is active, its outer(outside) layer rings are all active
- If a ring is inactive, all of its inner(inside) rings are inactive

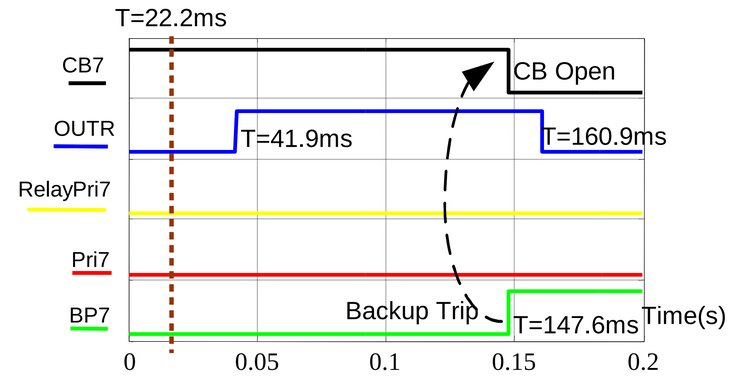


Results_1: ABG fault on Bus 4

Case1: Primary Protection



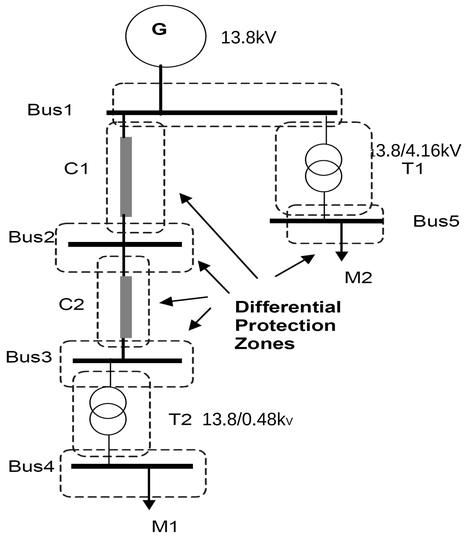
Case2: Backup protection



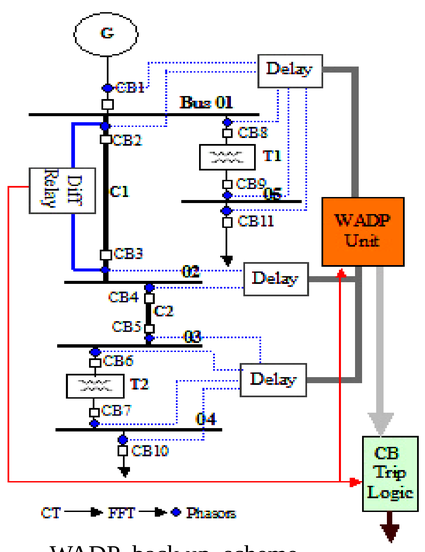
Signals:
CB7: Circuit Breaker7 Close/Open
OUTR: Outmost Ring Relay Trip
RelayPri7: Relay primary trip to CB7
Pri7: Confirmed Primary trip to CB7
BP7: Backup trip to CB7

1. Primary Protection Trip Sequence
   OUTR – RelayPri7 – Pri 7– CB7
2. Backup Protection Trip Sequence
   OUTR – BP7– CB7
3. Backup trips the same breakers as the primary

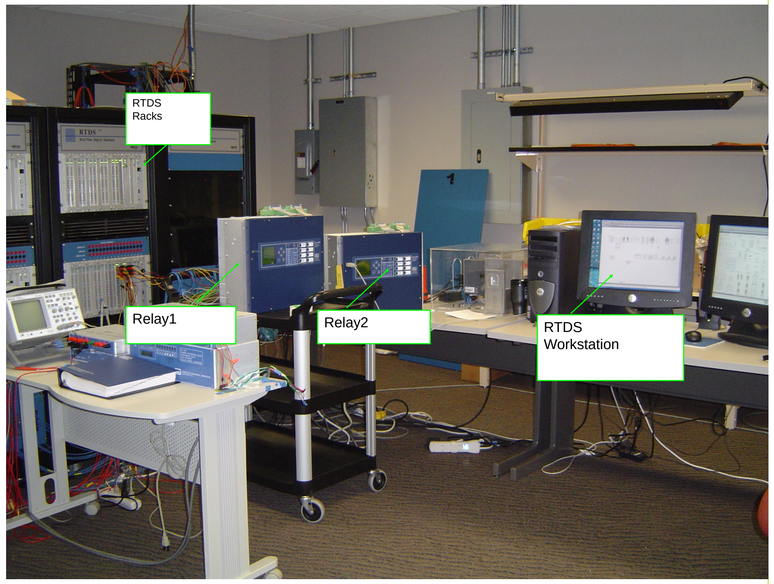
Microgrid System running on the RTDS showing protection zones



Conventional primary differential protection zones. Typical operating time 20ms



WADP back up scheme.
Typical operating time around 100ms +.



RTDS racks running the real time power system simulation and the hardware relays performing the conventional primary protection.

The back-up algorithm was performed on a relay emulated on RTDS hardware (DSP)

Primary protection done by local conventional relay hardware. The local hardware produces time tagged phasors for transmission to the collection center for wide area back-up protection.
Back-up protection algorithm will be run at the remote site where phasors are collected.

The communication system was not simulated in this preliminary study. An arbitrary delay of 100ms was inserted in the back-up loop to represent the time taken to collect the phasors and run the algorithm. Future work will include the communication system and deal properly with latency and delays.