

# Brief Overview of IEEE 1588 Test Results – Concept and Practical Examples and Lessons Learned

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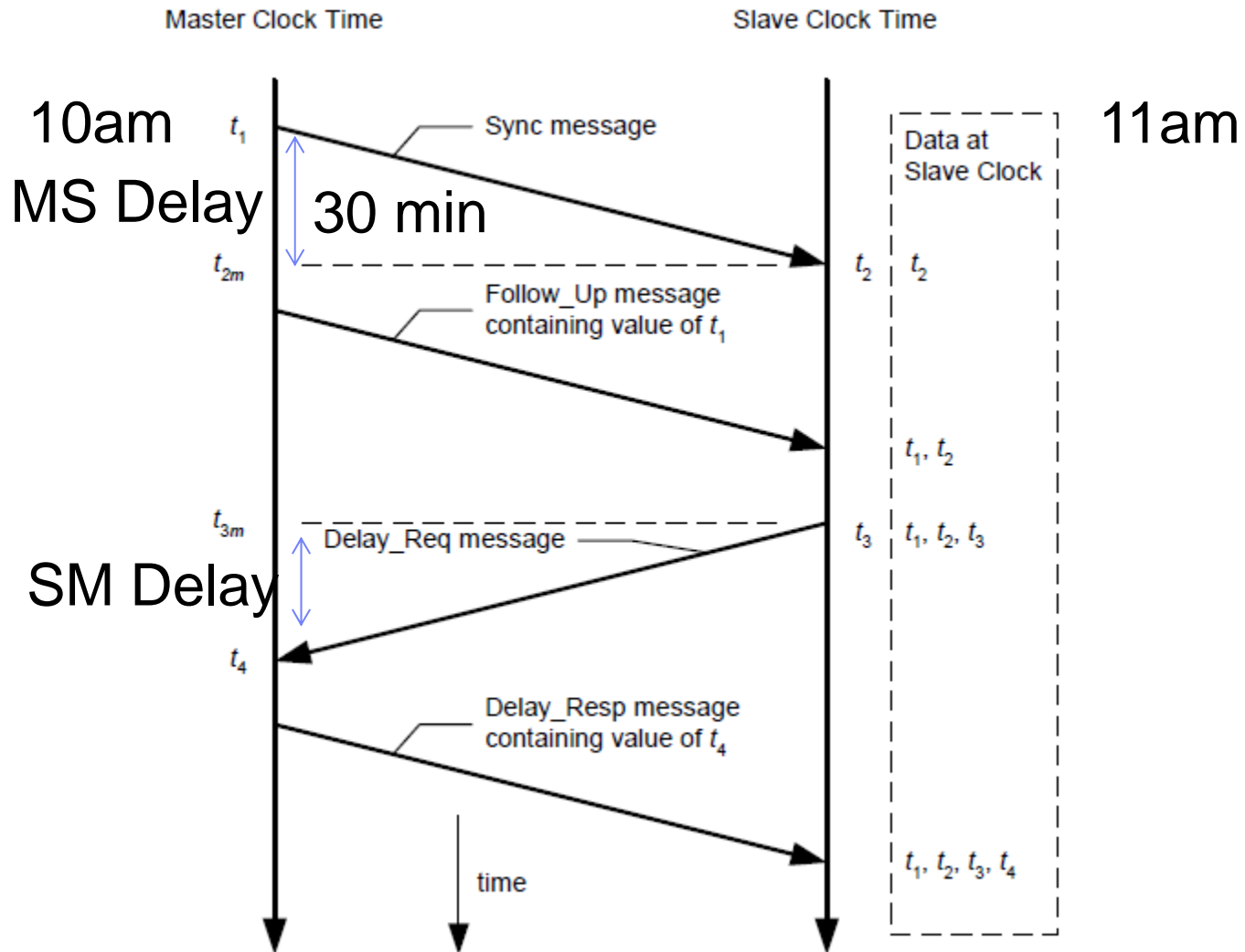
NASPI Meeting, October 16, 2012, Atlanta, GA



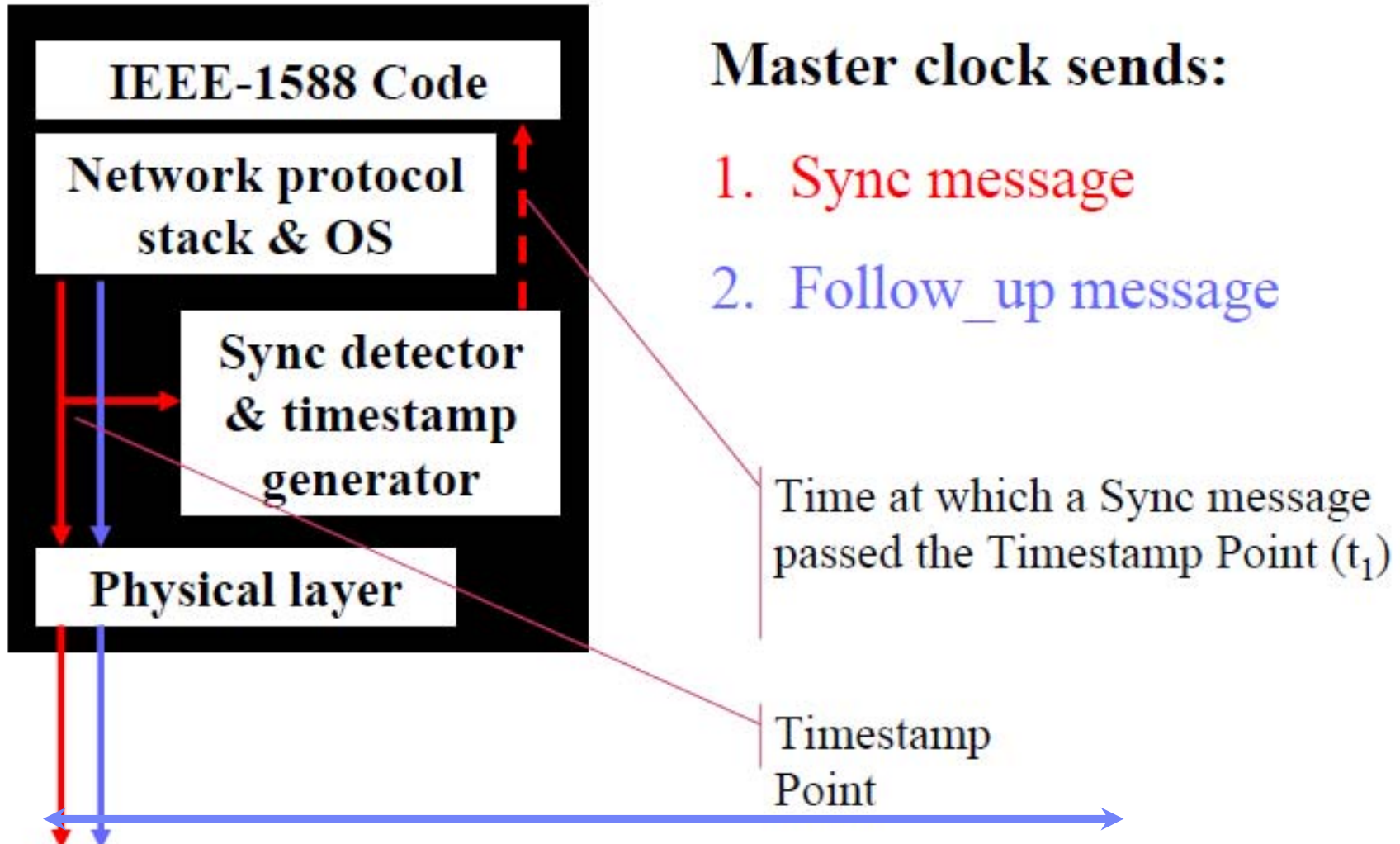
# IEEE 1588 – Precision Time Protocol (PTP) over Ethernet

- Capable of sub-microsecond time sync
- Provides a messaging system to identify the various clock performances
- Operates through messages in the Ethernet data frame

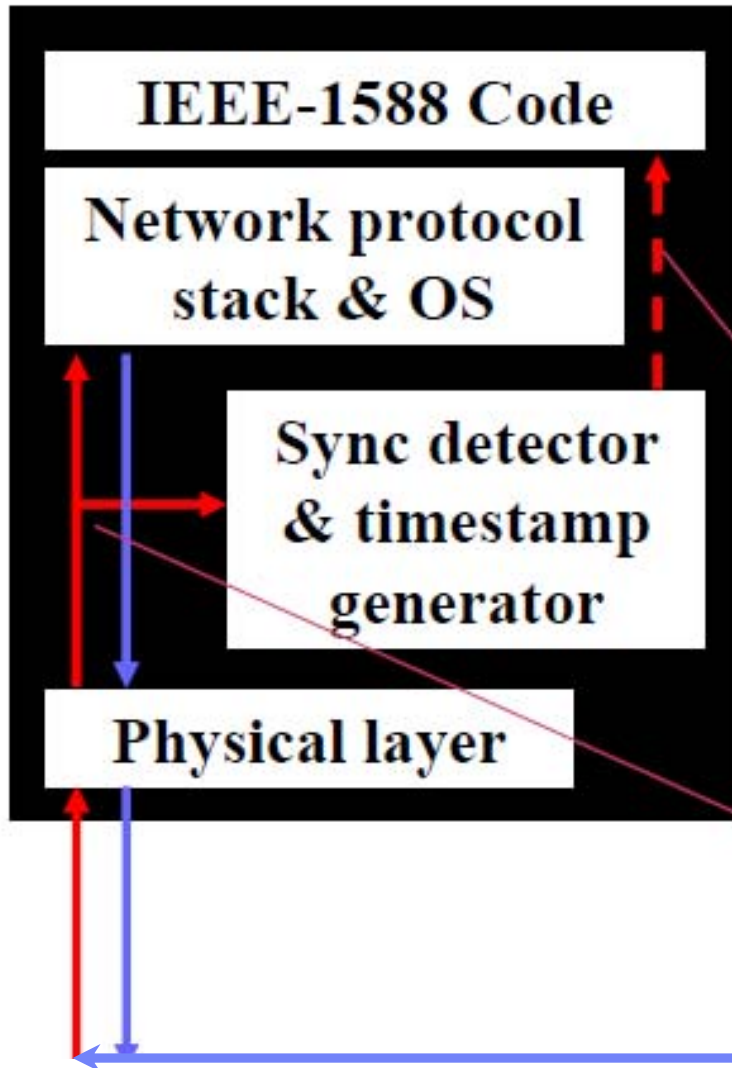
# 1588 Basic Operation (1-step, 2-step)



# Synchronization Details (clauses 6 & 7)



# Synchronization Details (continued)



**Master clock receives:**

- Delay\_Req message

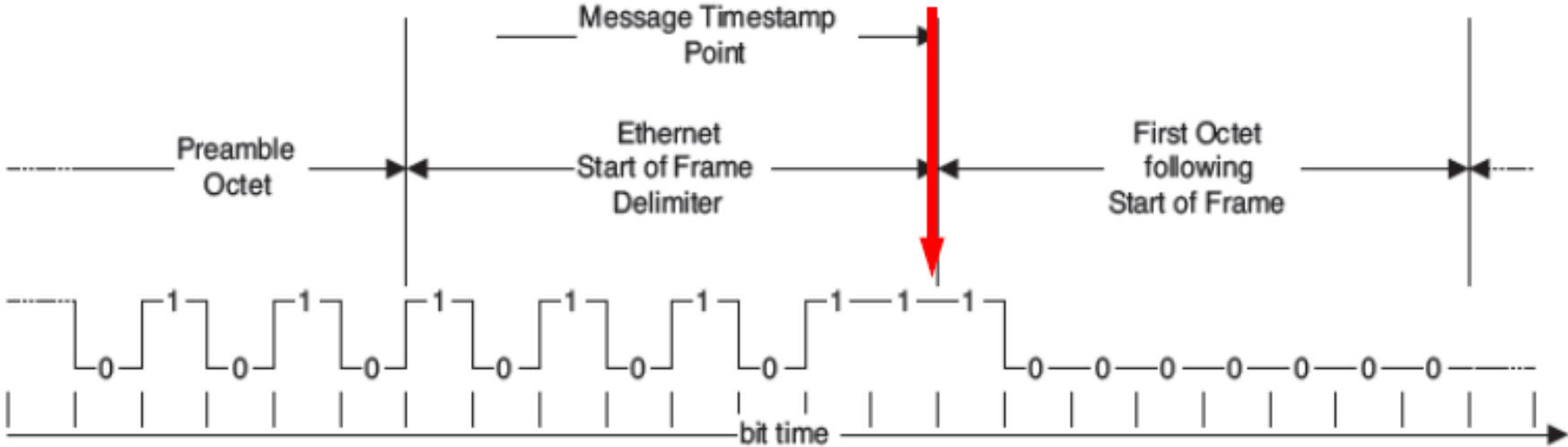
**Master clock sends:**

- Delay\_Resp message

Time at which a Delay\_Req message passed the Timestamp Point ( $t_4$ )

Timestamp Point

# Ethernet Message Time Stamping



Hardware-based Time Stamp is applied based on the Rising Edge of the First Bit after the Start of Frame Delimiter

# Time Sync Calculations

$$\begin{aligned} \text{MS\_difference} &= \text{offset} + \text{MS\_delay} = t_2 - t_1 \\ &= 11:30 - 10:00 = 90 \text{ min} \end{aligned}$$

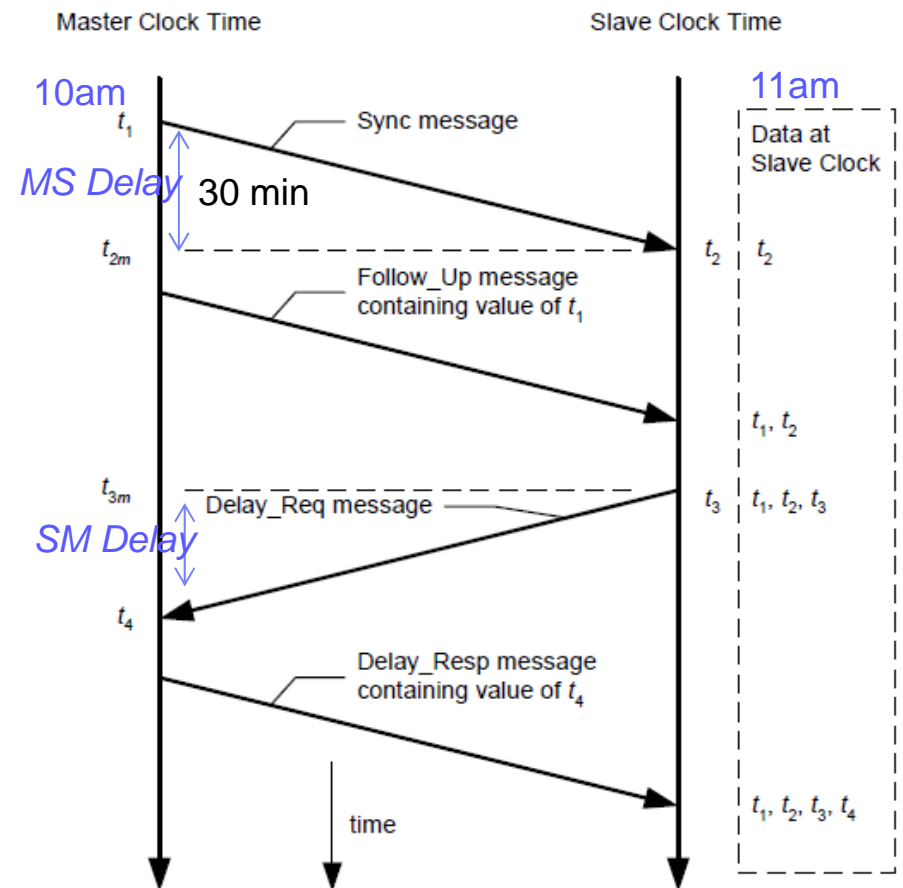
$$\begin{aligned} \text{SM\_difference} &= -\text{offset} + \text{SM\_delay} = t_4 - t_3 \\ &= 11:30 - 10:30 = -30 \text{ min} \end{aligned}$$

Assuming that MS\_delay=SM\_delay then:

## Offset and Delay Calculations

$$\begin{aligned} \text{Offset} &= (\text{MS\_difference} - \text{SM\_difference}) / 2 \\ &= (90 - (-30)) / 2 = 60 \text{ Min} \end{aligned}$$

$$\begin{aligned} \text{One\_Way\_Delay} &= (\text{MS\_Difference} + \text{SM\_difference}) / 2 \\ &= (90 + (-30)) / 2 = 30 \text{ min} \end{aligned}$$



## Announce Message:

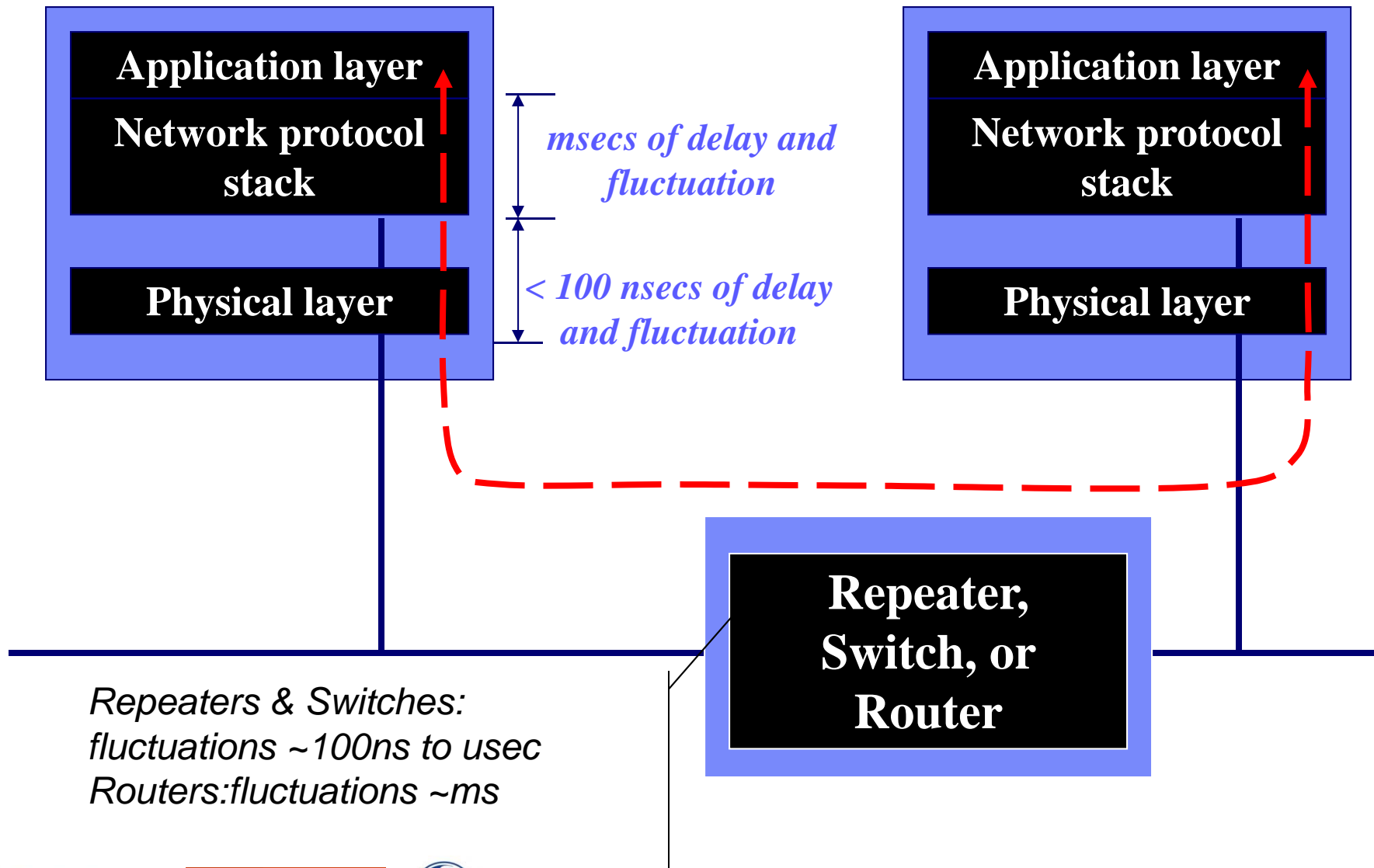
- Clock ID
- Grand Master Clock Accuracy
- Grand Master Variance
- Origin Time Stamp (Sec and nsec)
- UTC Offset
- Grand Master Time Source (e.g. – GPS)



## Included in the Sync Message:

- Message ID (e.g. – Sync, Follow-up, delay request)
- PTP Version Number
- Message Length (2 bytes)
- Subdomain Number (1 byte)
- PTP Flags (16)
- Correction (nsec)
- Clock Identity (8 bytes)
- Source Port (2 bytes)
- Origin Time Stamp (Seconds & Nanoseconds)

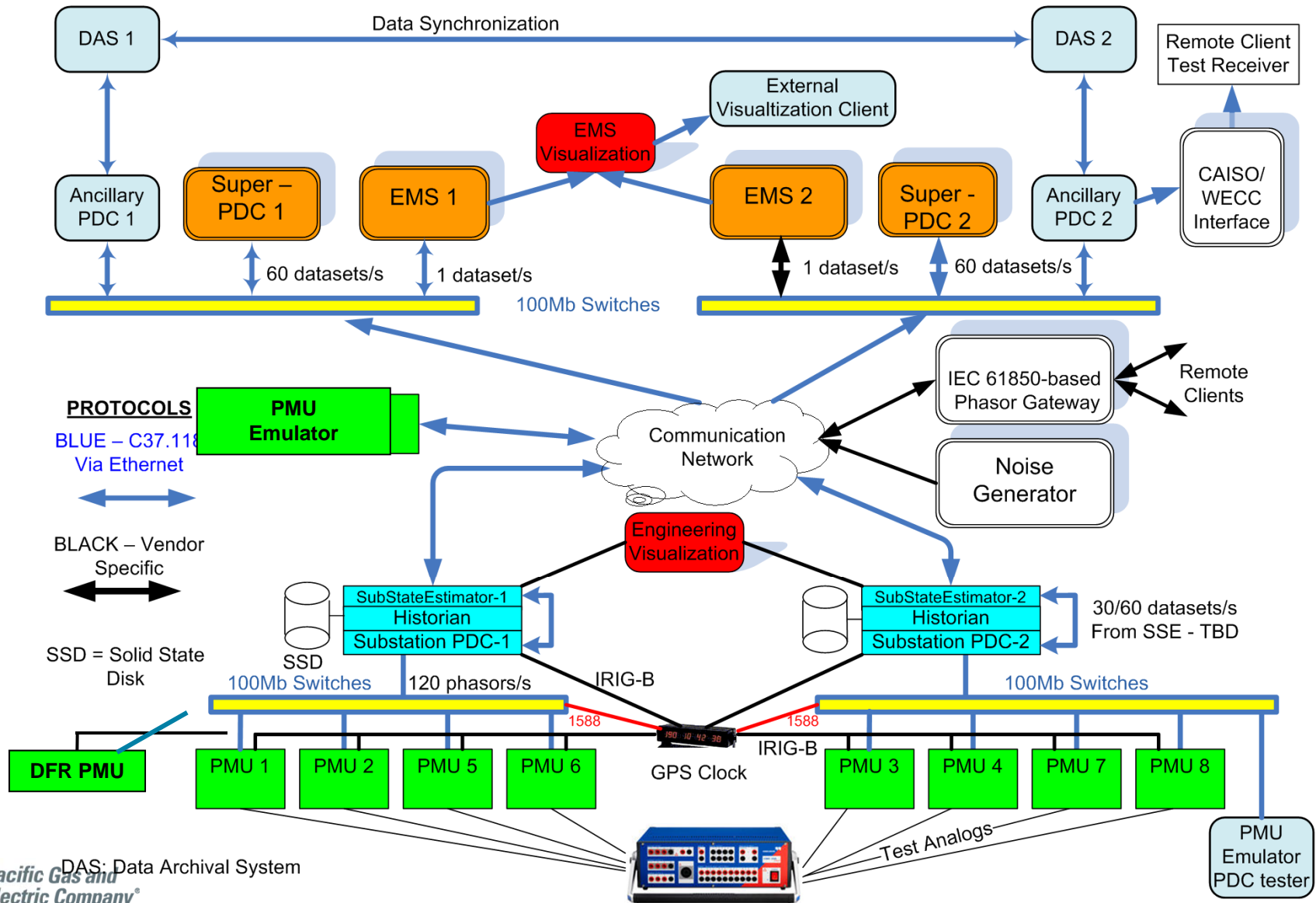
# Timing Latency & Fluctuation



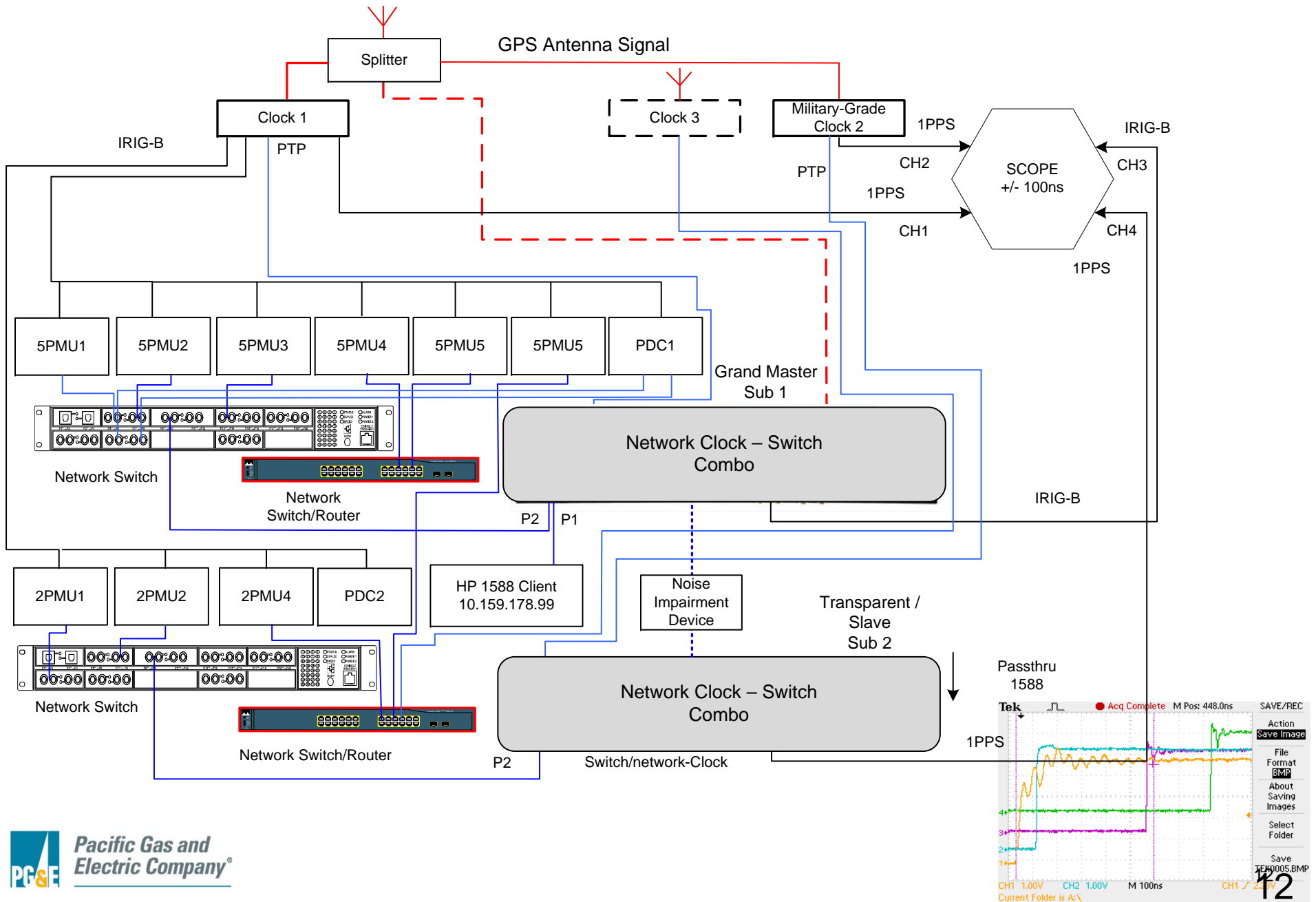
# Proof of Concept Testing - Architecture

## PG&E Synchrophasor Project – Proof of Concept Architecture

C37.118 is used for interim testing while harmonization with IEC 61850 is demonstrated



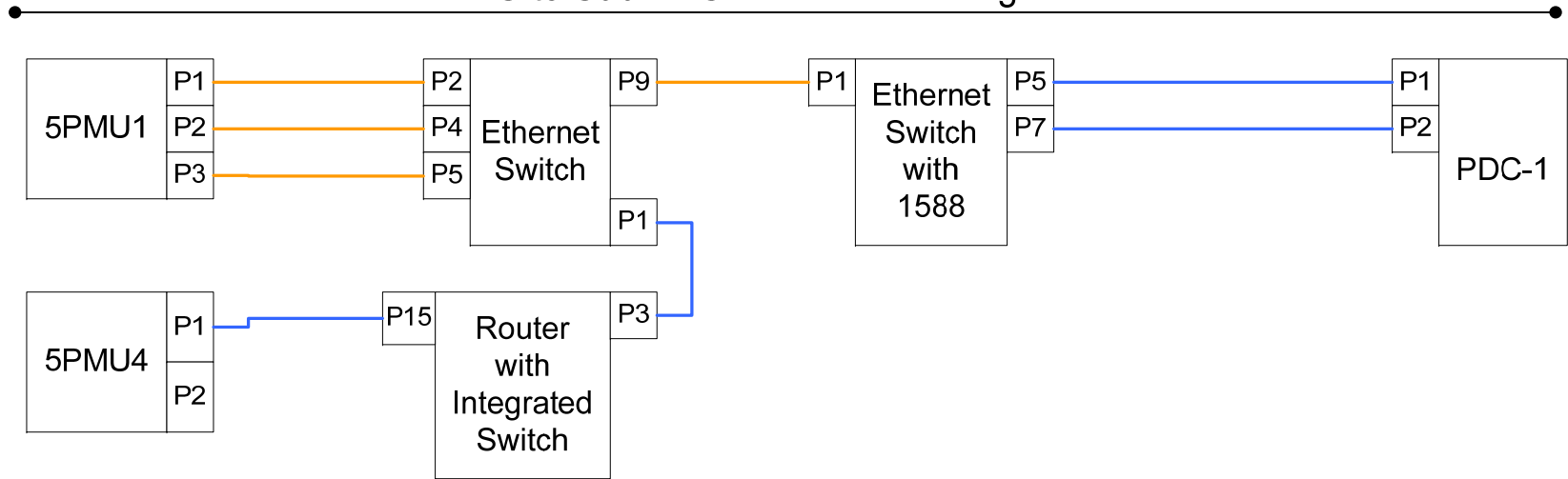
# Observations – Timing functions (GPS, IRIG-B, and IEEE 1588)



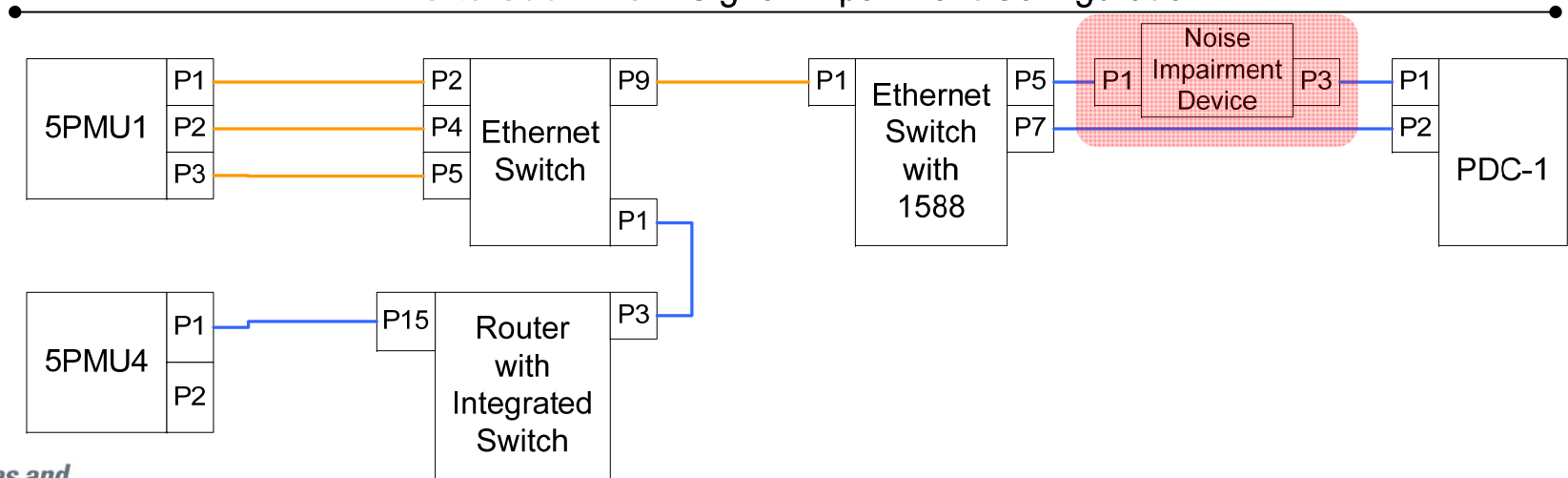
# Noise Impairment Tests

- Noise Injection / IP Packet interference

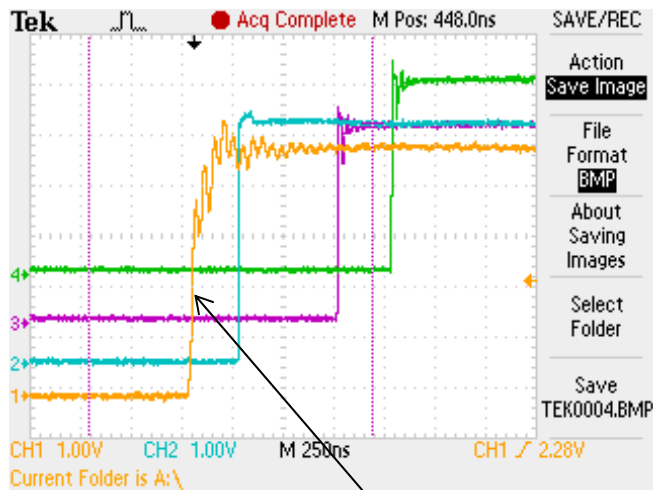
PMU to Sub PDC - Standard Configuration



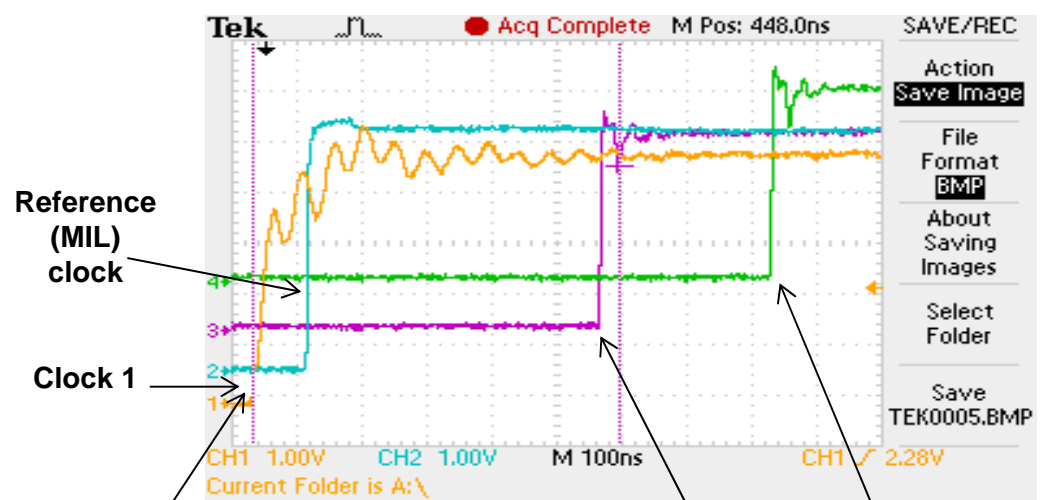
PMU to Sub PDC – Signal Impairment Configuration



# Observations – Timing functions (GPS, IRIG-B, and IEEE 1588)

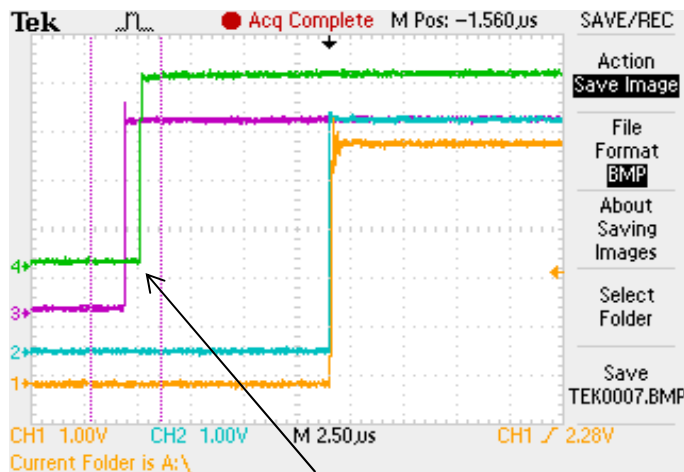


Before calibration (-0.25  $\mu$ s)

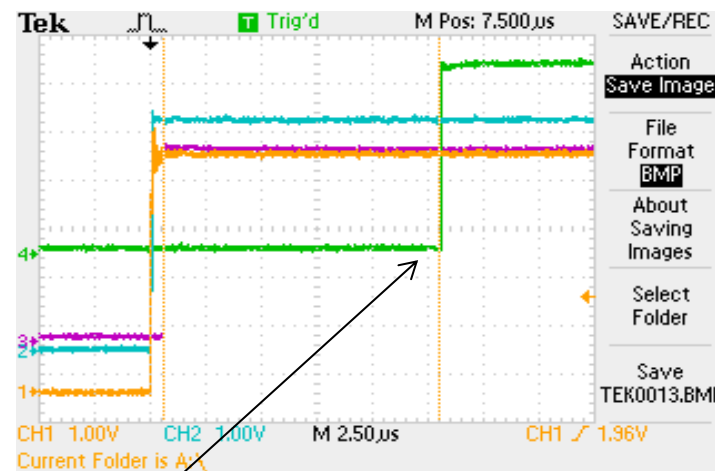


After calibration ( 0.1 $\mu$ s)  
Compensating for GPS  
Antenna cable length

Grandmaster Transparent-Clock



~15 minutes after GPS Antenna removal  
from Grandmaster(10  $\mu$ s)



10  $\mu$ s delay injected in 1588 path  
between grandmaster and transparent clock

## Observations – Timing functions (GPS, IRIG-B, and IEEE 1588)

- Several GPS-synchronized clocks providing timing accuracy better than 1 us (mostly on the order of 0.1 us)
- Some clocks did not update time-quality bits in IRIG-B timing data after loss of GPS input. Similarly, for IEEE 1588 PTP.
- In the absence of GPS input, clock drifts on the order of  $10^{-7}$  to  $10^{-9}$  were observed from different clocks.
  - Typical commercial products
    - $10^{-9}$  is a drift of 4 us in about an hour
    - $10^{-7}$  is a drift of 26 us in about 4 minutes (Bad Time)
      - Synchrophasor permissible TVE of 1% ~ 26.5 us
- Other 1588 PTP (precision time protocol) test results
  - Typical accuracy of 0.1 to 0.5 us has been observed.
  - Any delay in network communication can translate to delay in Transparent Clock when not compensated.
  - Some Slave clocks assume transmission delay is the same in both directions (usually OK, but not always)

# Tests – Summary of the Findings

- Several GPS-synchronized clocks providing timing accuracy better than 1 us (mostly on the order of 0.1 us)
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# IEC61850 Levels of Time Synchronization

LN – STIM identified to set time and provide time synchronization in a substation

<u>Class</u>	<u>Accuracy</u>	<u>Function/phase error</u>
T1	$\pm 1$ ms	Event timing
T2	$\pm 0.1$ ms	Zero Crossing / Sync Check
T3	$\pm 25$ $\mu$ s	32' at 60Hz / 27' at 50 Hz
T4	$\pm 4$ $\mu$ s	5' at 60Hz / 4' at 50 Hz
T5	$\pm 1$ $\mu$ s	1' - Synchrophasors
T6	$\pm 0.1$ $\mu$ s	Available, but not defined yet

## C37.118 4 Bit Time Quality Indicator Code

BINARY	HEX	VALUE (worst case accuracy)
1111	F	Fault--Clock failure, time not reliable
1011	B	10 seconds
1010	A	1 second
1001	9	100 milliseconds (time within 0.1 sec)
1000	8	10 milliseconds (time within 0.01 sec)
0111	7	1 millisecond (time within 0.001 sec)
0110	6	100 microseconds (time within $10^{-4}$ sec)
0101	5	10 microseconds (time within $10^{-5}$ sec)
0100	4	1 microsecond (time within $10^{-6}$ sec)
0011	3	100 nanoseconds (time within $10^{-7}$ sec)
0010	2	10 nanoseconds (time within $10^{-8}$ sec)
0001	1	1 nanosecond (time within $10^{-9}$ sec)
0000	0	Normal operation, clock locked